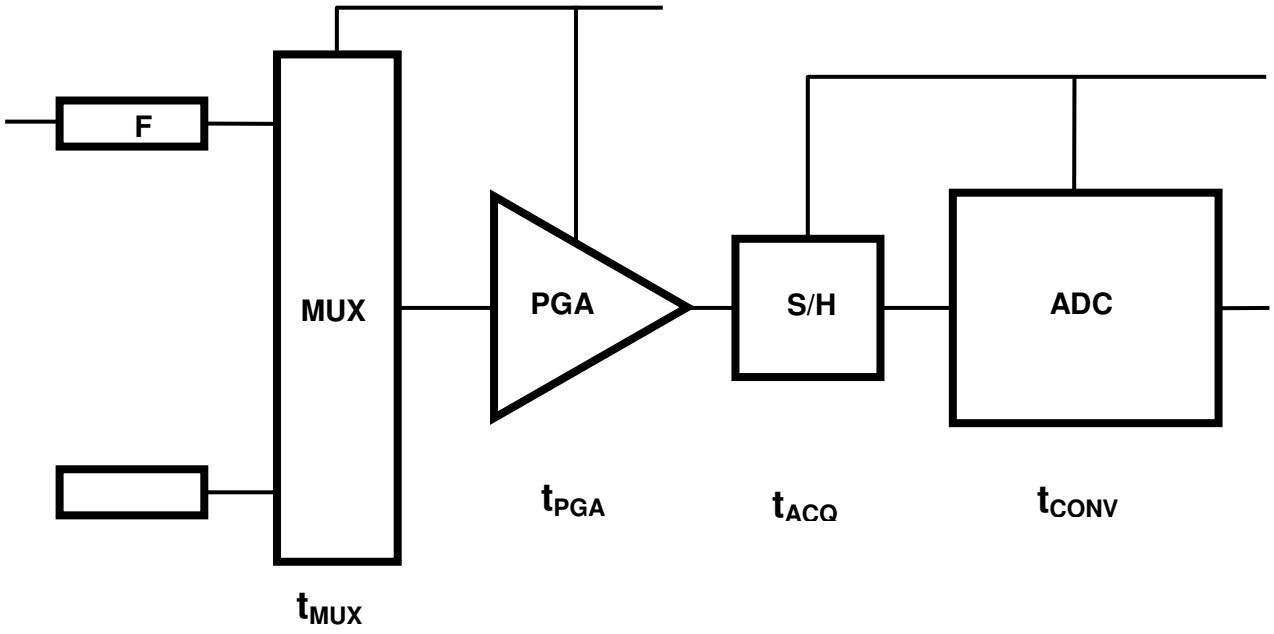
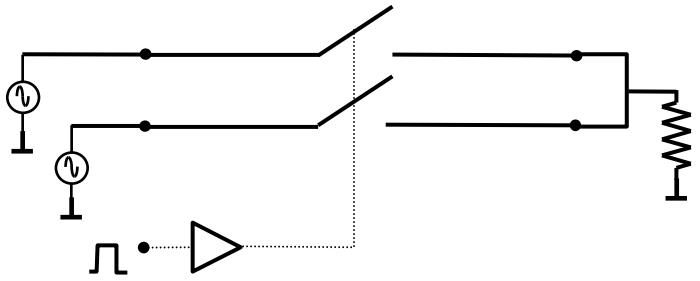
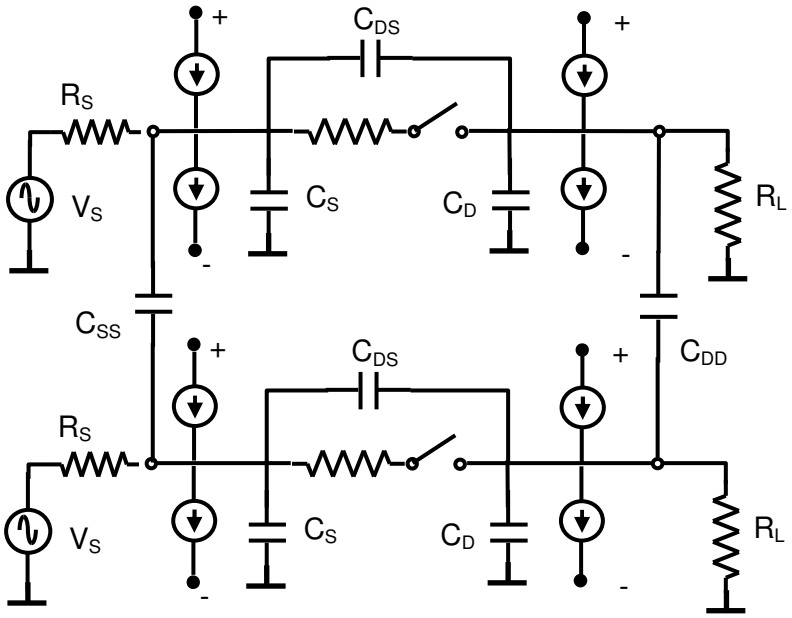
CONVERTIDORES A/D – D/A.

SISTEMA DE ADQUISICIÓN:



LLAVES ANALÓGICAS / MULTIPLEXERS





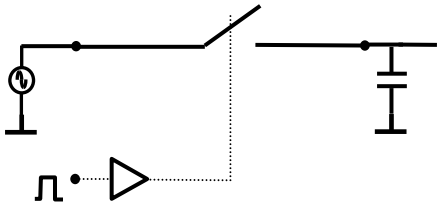
Errores estáticos:

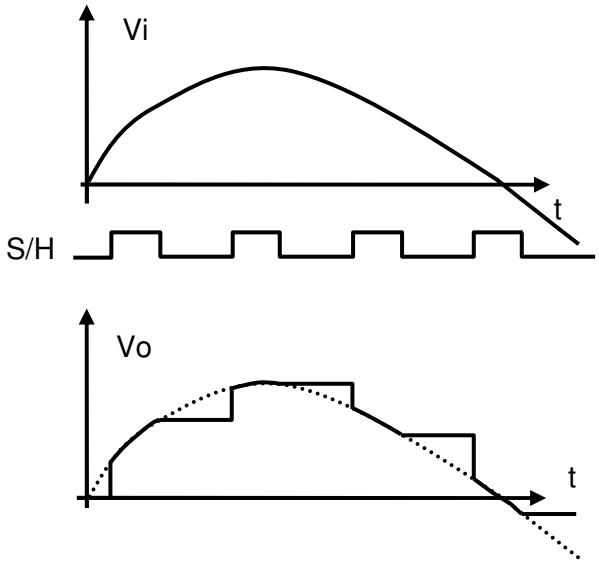
R_{on}
$\triangle R_{on}$
I_I

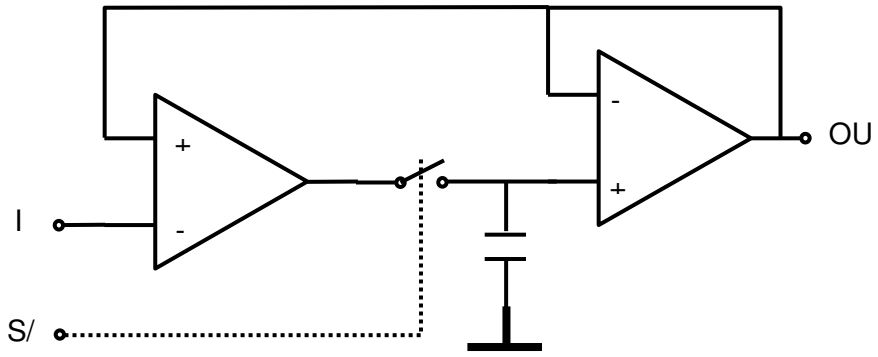
Errores dinámicos:

t_{on}, $t_{off,}$ $\triangle t_{on}$, $\triangle t_{off}$
Charge injection
Crosstalk

Sample – hold

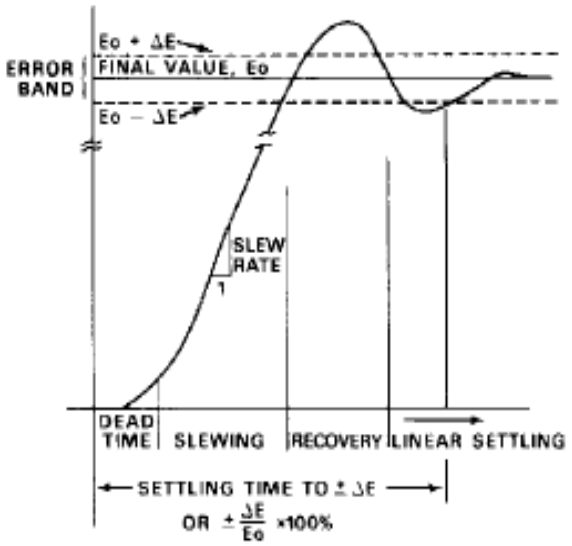






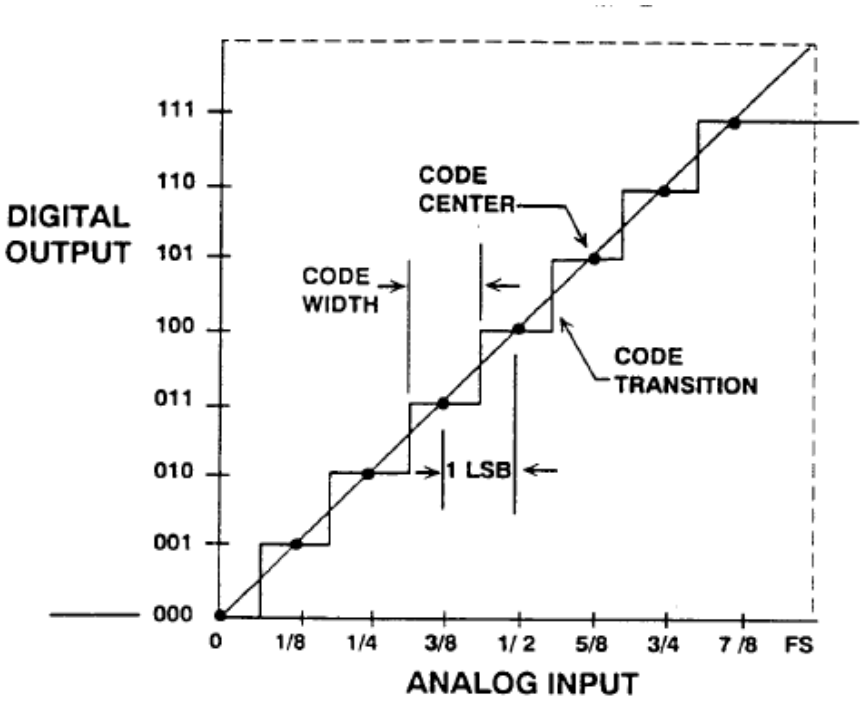
Errores estáticos:

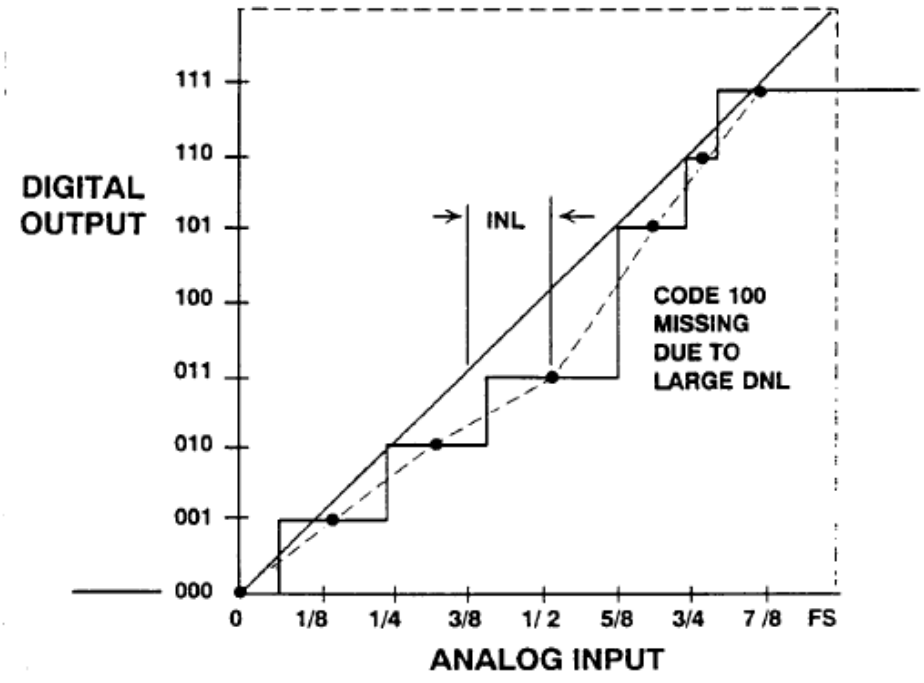
R_{on}
R_s
R_L



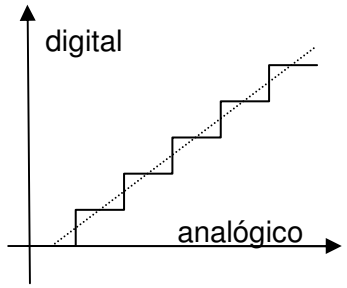
Errores dinámicos:
settling time
aperture uncertainty
charge injection
droop error

CONVERSIÓN ANALÓGICO - DIGITAL



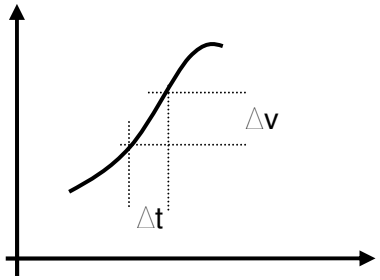


ERROR DE CUANTIZACIÓN



$$e_q = \sqrt{\frac{1}{q}\int_{-q/2}^{q/2} v^2 dv} = \frac{q}{\sqrt{12}}$$

ERROR DE FASE:



$$v = A \cdot \text{sen } \omega t \qquad \frac{\text{dv}}{\text{dt}}\Big|_{t=0} = \omega \cdot A$$

$$\Delta v = 2\pi f \cdot A \cdot \Delta t$$

Relación señal a ruido para una sinusoide

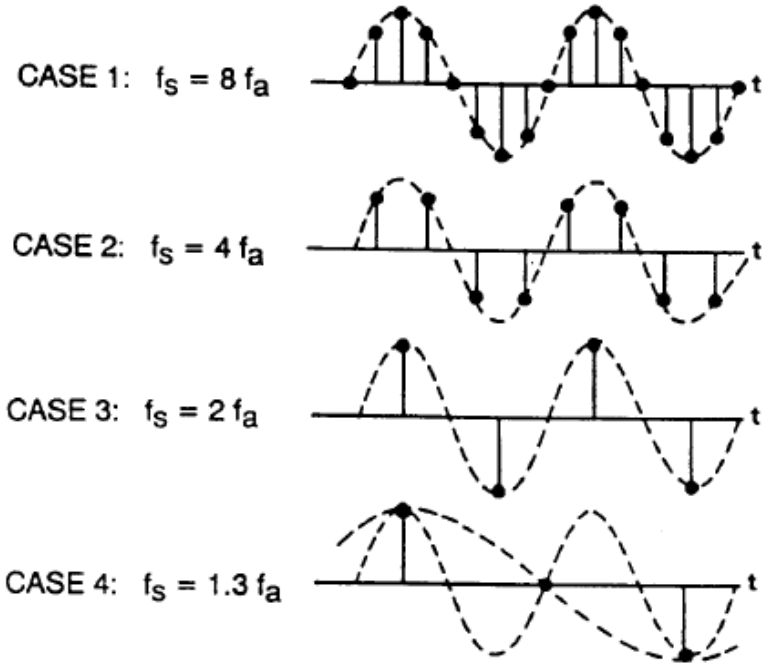
$$\frac{S}{N} = \frac{\frac{2^N \cdot q}{2\sqrt{2}}}{\frac{q}{\sqrt{12}}} = 2^N \frac{\sqrt{12}}{2\sqrt{2}}$$

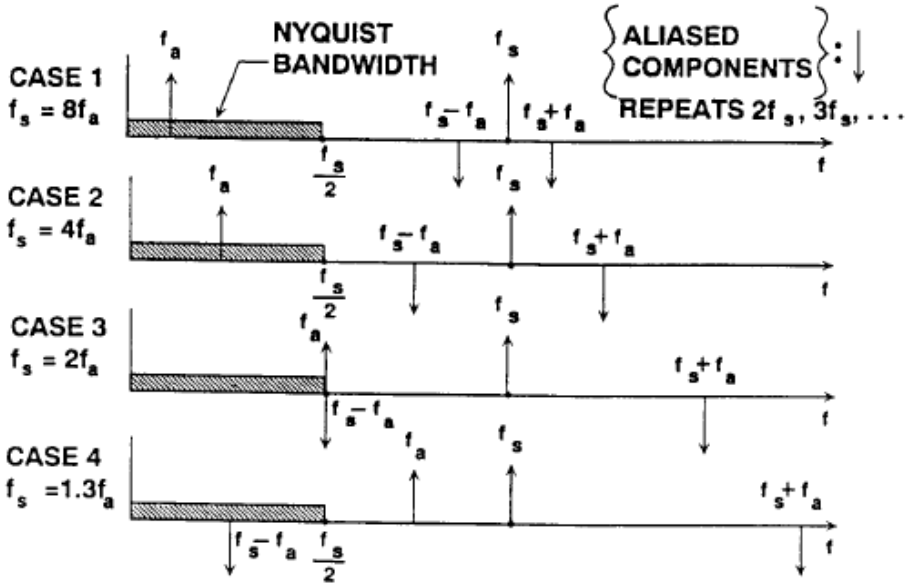
$$\frac{S}{N}[db] = N \cdot 20 \log 2 + 20 \log \frac{\sqrt{6}}{2}$$

$$\frac{S}{N} = 6,02 \cdot N + 1,76[db]$$

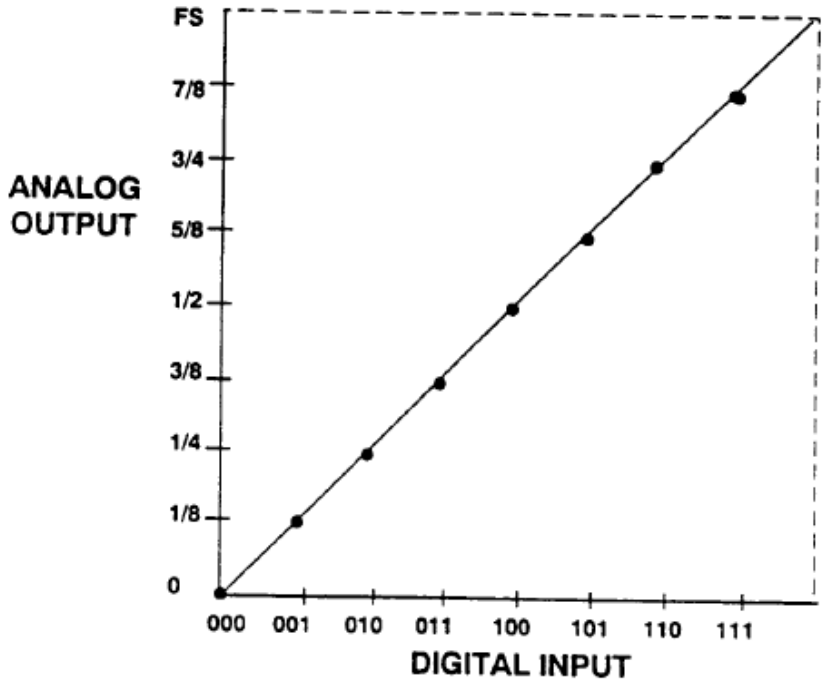
$$\text{ENOB} = \frac{\text{SNR(total)}}{6,02} - 1,76$$

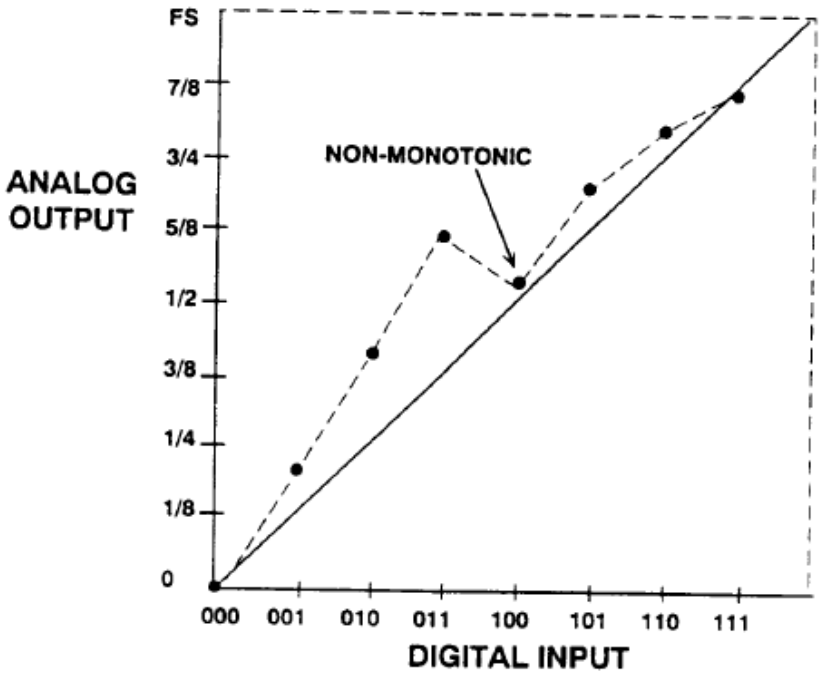
Frecuencia de muestreo



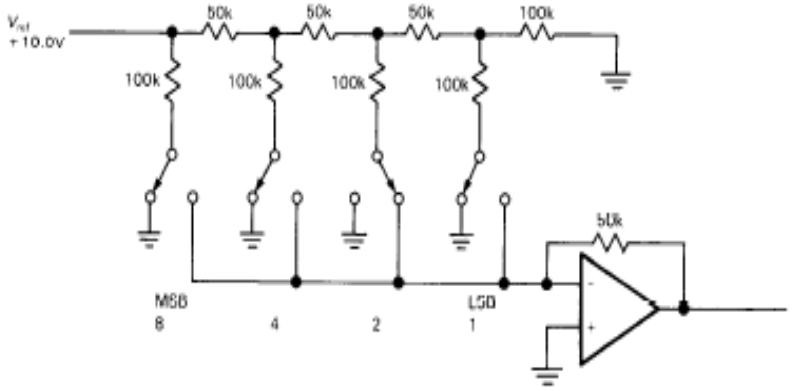


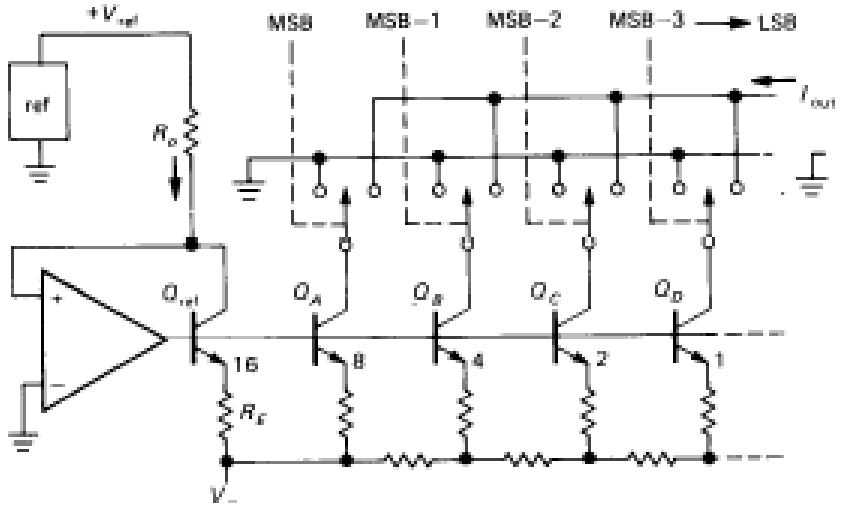
Conversión digital - analógica



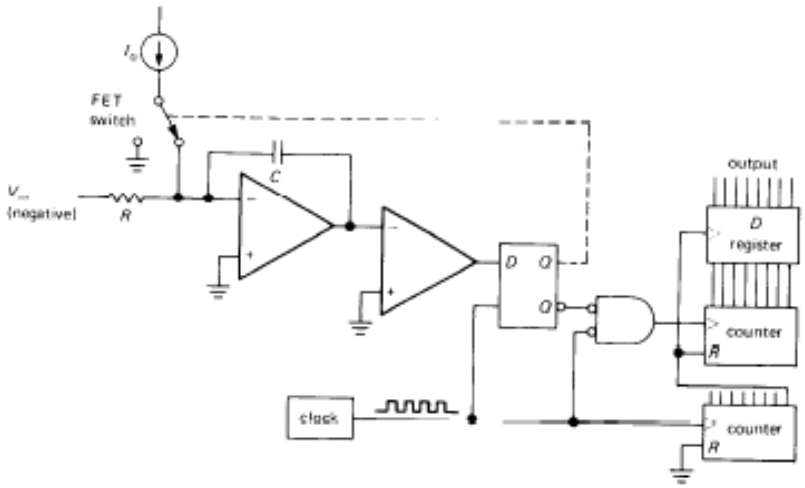


ALGUNAS IMPLEMENTACIONES DE CONVERTIDORES D/A





ALGUNAS IMPLEMENTACIONES DE CONVERTIDORES A/D



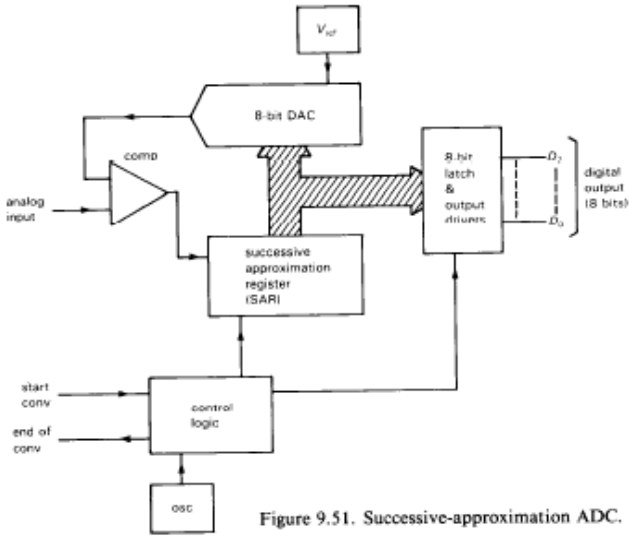


Figure 9.51. Successive-approximation ADC.

CONVERTIDOR SIGMA / DELTA.

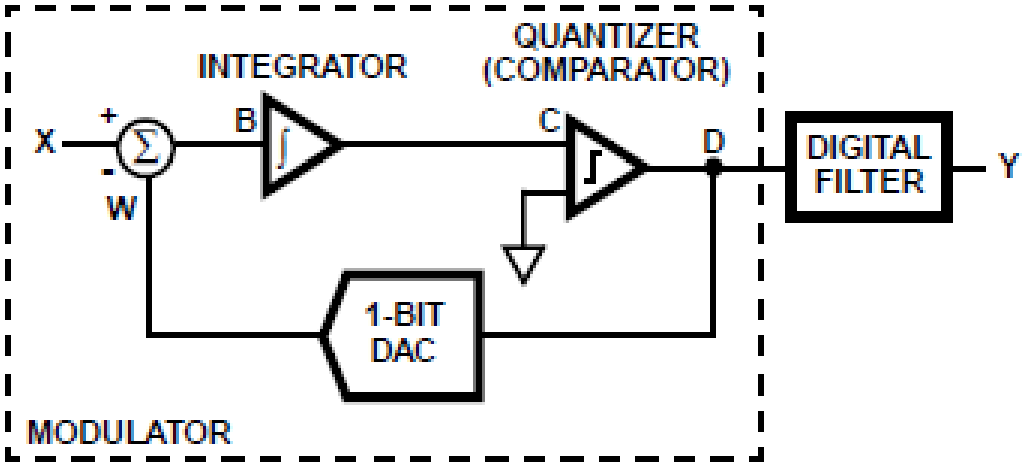


FIGURE 1. FIRST ORDER SIGMA DELTA ADC BLOCK DIAGRAM

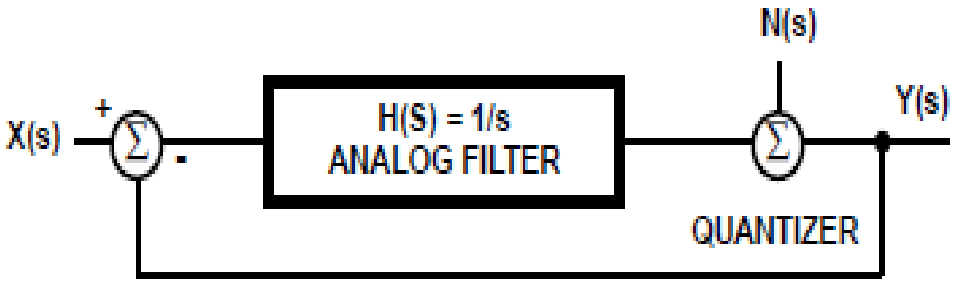


FIGURE 8. LINEARIZED MODEL OF 1ST ORDER SIGMA DELTA MODULATOR

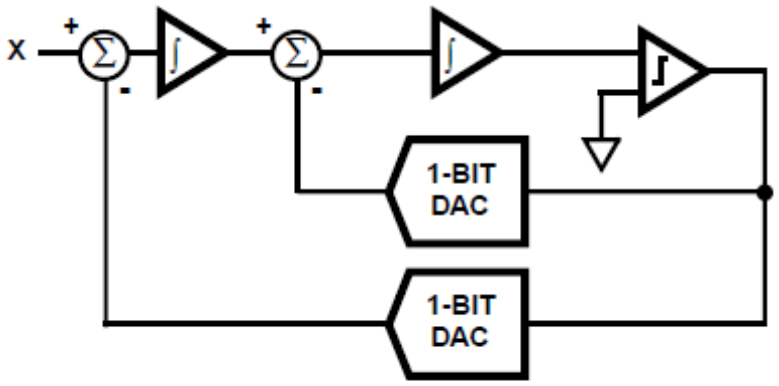


FIGURE 5. SECOND ORDER SIGMA DELTA MODULATOR

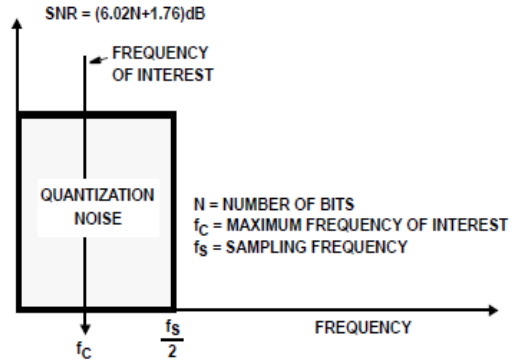


FIGURE 7A. NYQUIST CONVERTER QUANTIZATION NOISE SPECTRUM

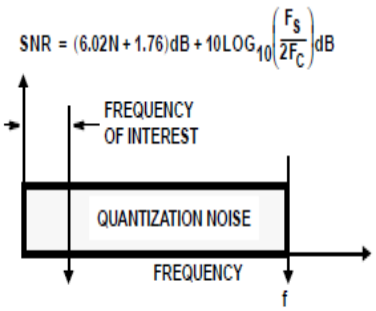


FIGURE 7B. OVERSAMPLED CONVERTER QUANTIZATION NOISE SPECTRUM

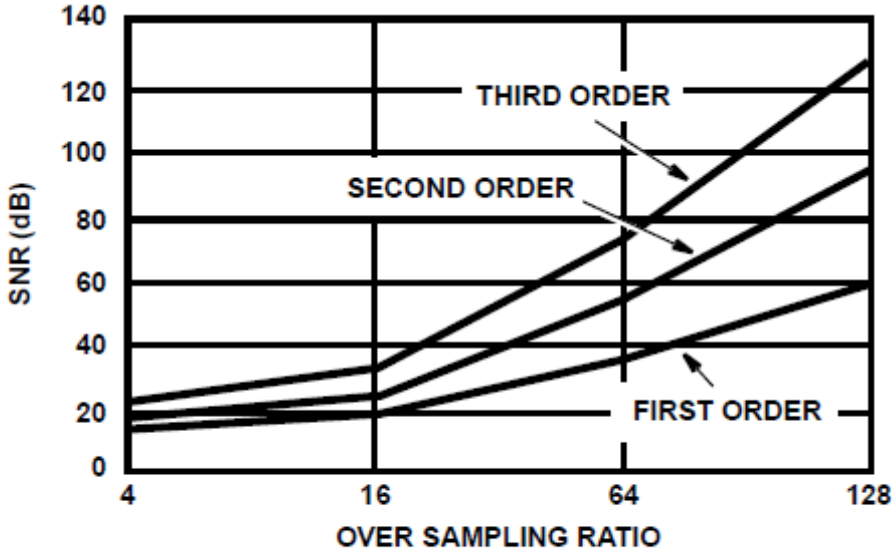
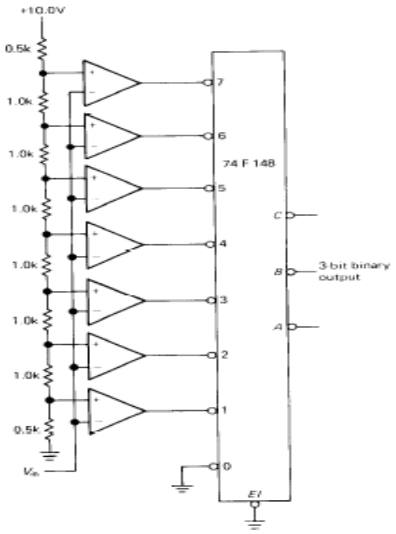


FIGURE 6. SNR vs OVERSAMPLING RATIO FOR SIGMA DELTA MODULATORS

FLASH



FLASH CONVERTER HISTORICAL PERSPECTIVE

The first documented flash converter was part of Paul M. Rainey's electro-mechanical PCM facsimile system described in a relatively ignored patent filed in 1921 (Reference 5). In the ADC, a current proportional to the intensity of light drives a galvanometer which in turn moves another beam of light which activates one of 32 individual photocells, depending upon the amount of galvanometer deflection. Each individual photocell output activates part of a relay network which generates the 5-bit binary code as shown in Figure 6.

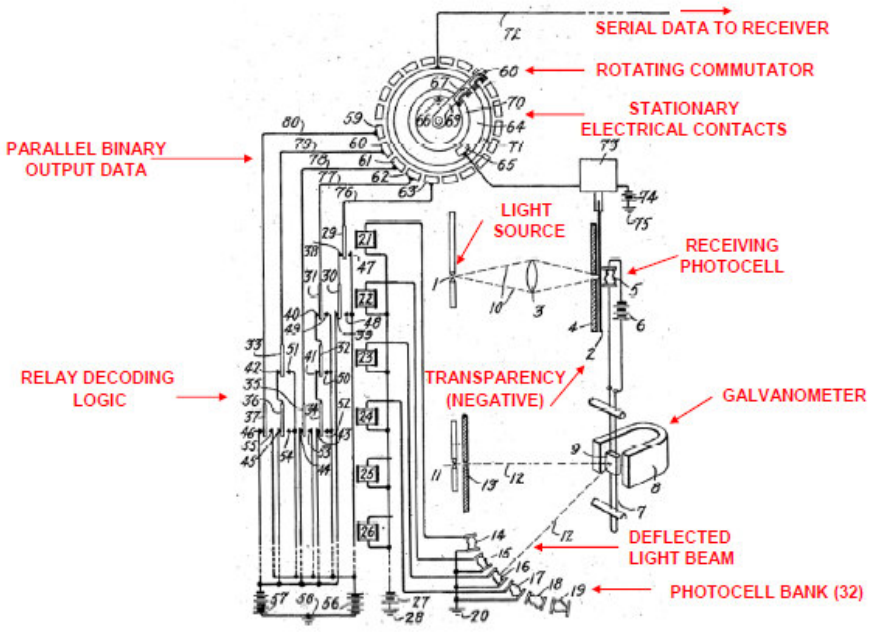


Figure 6: A 5-Bit Flash ADC Proposed by Paul Rainey
Adapted from Paul M. Rainey, "Facsimile Telegraph System," U.S. Patent 1,608,527, Filed July 20, 1921, Issued November 30, 1926

A significant development in high speed ADC technology during the 1940s was the electron beam coding tube developed at Bell Labs and shown in Figure 7. The tube described by R. W. Sears in Reference 6 was capable of sampling at 96 kSPS with 7-bit resolution. The basic electron beam coder concepts are shown in Figure 6 for a 4-bit device. The tube used a fan-shaped beam creating a "flash" converter delivering a parallel output word.